UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/392,865	09/09/99	KITAMURA S	005702-20035

MM91/0622

WILLIAM H. WRIGHT, ESQ.
HOGAN & HARTSON, L.L.P.
BILTMORE TOWER
500 SOUTH GRAND AVENUE , SUITE 1900
LOS ANGELES CA 90071-4164

EXAMINER	
TRAN, T	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 06/22/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/392,865	KITAMURA ET AL.	
	Examiner	Art Unit	
	Thien F Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-7,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☐ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 17 is objected to because of the following informalities: line 13, "said element separate regions" should be --said element separating regions--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 17 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The recitation of each of the floating gates not being formed on the element separating regions can be interpreted as setting forth structure not supported by the disclosure. The disclosure (see Fig. 3a) clearly shows portions of floating gates 4 being formed on the element separating regions 2. Also, the recitation in each the element separating region, both the oxide film and the another oxide film being formed between each the side wall and each the floating and control gates can be interpreted as setting forth structure not supported by the disclosure. The disclosure shows in the element separating region (see Fig. 11b), both the oxide

film 31 and the another oxide film 32 being formed between the side wall 10 and the control gate 6 but not between the side wall 10 and the floating gate 4.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 17 recites the limitation "said memory regions" in line 10, line 12 and line 14. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5, 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al. (US 5,068,697) in view of Reference U (TDB-ACC-NO: NN8801295) or Chau et al. (US 5,434,093) or Bracchitta et al. (US 5,518,945).

Noda et al. discloses a nonvolatile semiconductor memory device (Fig. 4) comprising a semiconductor substrate 21; memory transistors formed on said semiconductor substrate to

perform nonvolatile storage of an electric charge in accordance with data, each of said memory transistors being an electrically rewritable memory transistor including a floating gate FG formed over said semiconductor substrate via a first gate insulating film 23 and a control gate CG formed over said floating gate via a second gate insulating film 24; an oxide film (23, 25) formed on said substrate and at least on both sides of each said floating gate and both sides of each said control gate; side walls 26 each for protecting sides of said floating gate and said control gate of each said transistor, each said side wall formed of PSG; a second silicon nitride film 29 covering surfaces of said control gate, a source diffusion layer 27, a drain diffusion layer 28 and each of said side walls of each of said memory transistors; and a wiring layer 32 formed over said second silicon nitride via an interlayer insulating film 30. Noda et al. does not disclose side walls 26 formed of LPCVD silicon nitride. Phosphorus silicate glass (PSG) and LPCVD silicon nitride are dielectric materials known in the art and routinely used to form protective side wall spacers in semiconductor device as shown for example by Reference U, Bracchitta et al. and Chau et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select either one of these materials as a suitable dielectric material for the protective side walls of Noda et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416. In fact, Chau et al. discloses other materials suitable for constructing spacers may be used in place of or in conjunction with the oxide spacer including nitride, BSG and PSG (col. 9, lines 31-37).

Bracchitta et al. discloses LPCVD nitride being used as spacers over the oxide 22 (Figs. 5-6); and Reference U (TDB-ACC-NO: NN8801295) also discloses LPCVD nitride being used as spacers 23 over the oxide 22 (see Fig. 2). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to substitute the PSG material of the side walls (spacers) 26 with the LPCVD nitride material as taught by Bracchitta et al. or Reference U so the nitride spacers are in intimate contact with the oxide covered gate and an effective contamination barrier is formed to block mobile ions from invading the gate region.

Regarding claim 5, the modified Noda et al. does not explicitly disclose metal silicide films formed on the surfaces of said control gate, said source/drain diffusion layers of each of said transistors. It is conventional to form metal silicide films on a control gate surface and on surfaces of source/drain regions to reduce contact resistance. Therefore, the incorporation of the conventional features into the modified Noda et al. would have been prima facie obvious.

Regarding claim 6, as a result of the incorporation of said metal silicide films on the surfaces of said source/drain diffusion layers (27, 28), the modified Noda et al. discloses said drain diffusion layer connected to a bit line 32 via said metal silicide film and said source diffusion layer connected to a source line 31 via the metal silicide film respectively. The modified Noda et al. does not disclose the source line 31 is a common source line. However, it is old and well known in the art to form a common source line connecting source diffusion layers of adjacent memory transistors together. Therefore, forming the source line 31 as a common source line for the adjacent memory transistors would have been prima facie obvious.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al. (US 5,068,697) in view of Reference U (TDB-ACC-NO: NN8801295) or Chau et al. (US 5,434,093) or Bracchitta et al. (US 5,518,945) as applied to claims 5, 6 and 16 above, and further in view of Santin et al. (US 5,907,171).

The modified Noda et al. as described above does not explicitly disclose at least one of a low-voltage MOS transistor and a high-voltage MOS transistor formed as a peripheral circuit. It is conventional to form low-voltage transistor and high-voltage transistor as a peripheral circuit of a memory array, as shown for example by Santin et al. Therefore, the incorporation of the conventional features into the modified Noda et al. would have been prima facie obvious.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Thien Tran** whose telephone number is (703) 308-4108. The examiner can normally be reached on Monday through Friday from 7:30AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt

June 19, 2001

Sara Crane
Primary Examiner